**ECE 324 Homework5: FIFO simulation**

Name: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

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| **Exercise** | **Course outcome** | | **Grade** |
| Homework5 | | 2.a, 7.b | /30 |

2.a. Define engineering problems from specified needs for digital systems including implementation on FPGAs using HDL programming.

7.b. Employ appropriate learning strategies such as communicating with an expert, using external resources, experimentation, simulation, etc.

# Exercise

Use Chu’s fifo.sv, reg\_file.sv, and fifo\_ctrl.sv (modified) in the following:

1. Add another design assertion to fifo\_ctrl.sv (leveraged from Chu) which displays an error message if the FIFO were ever to be both full and empty at the same time.
2. Add another testbench assertion to fifo\_ctrl.sv which displays a warning message if the testbench were to cause the FIFO to overflow (write when the fifo is full).
3. To act as the device under test in a new SystemVerilog testbench module, instantiate Chu’s fifo module, making the fifo 8 words deep, with each word being 16 bits wide.
4. Complete your testbench to verify the FIFO functionality, and include both an underflow and an overflow.
5. Perform the simulation using Vivado, and confirm your results are correct, including the assertions for underflow and overflow.
6. Submit the following for grading by uploading it to the drop box on Blackboard:
   1. All SystemVerilog code, both functional module and testbench. The SystemVerilog code should include comments that explain how it works.
   2. Screenshots of simulation results (including any assertion outputs) proving that your module functions correctly. Make sure all signal names and time labels are legible.
   3. A written report that explains how your simulation results show that your module and testbench assertions function correctly. Please attach the provided cover sheet to your report.